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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,324	08/27/2001	Robert T. George	2207/12003	5090

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KENYON & KENYON (SAN JOSE)
333 WEST SAN CARLOS ST.
SUITE 600
SAN JOSE, CA 95110

EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,324	GEORGE ET AL.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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Detailed Action

1. Claims 1-17 are presented for examination. This office action is in response to the RCE filed on 8/13/04.

2. The 35 USC § 112 rejection to the claims has been withdrawn because of the Amendment.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-4, 6-12, and 14 are rejected under 35 U.S.C. 102(a) as being anticipated by Shen et al. (Shen) U.S. Patent 6,526,481.

As to claim 1, Shen discloses a cache-coherent I/O device (each cache is I/O by the Refs. 110) comprising (Fig. 2): a plurality of client ports (Fig. 2 Refs. Refs. 130's), each to be coupled to one of a plurality of port components (Fig. 2 Refs. 110); a plurality of sub-unit caches (Fig. 2 Refs. 134), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components; and a coherency engine (Fig. 2 Refs. 132 & 140) coupled to said plurality of sub-unit caches. However, Shen does not specifically disclose an integrated single cache coherent device.

As to claim 2, Shen discloses the invention as claimed in the above. Shen further discloses wherein said plurality of port components includes processor port components (Fig. 2 Ref. 110).

As to claim 3, Shen discloses the invention as claimed in the above. Shen further discloses wherein said plurality of port components includes input/output components (Fig. 2 Ref. 110).

As to claim 4, Shen discloses the invention as claimed in the above. Shen further discloses wherein said plurality of sub-unit caches includes transaction buffers using a coherency logic protocol (Fig. 2 Refs. 132 & 140).

As to claim 6, Shen discloses a cache-processing system comprising (Fig. 2): a processor (Fig. 2 Ref 110); a plurality of port components (Fig. 2 Ref. 110); and a cache-coherent I/O device (Fig. 2 Refs. 132 & 140) coupled to said processor and including a plurality of client ports (Fig. 2 Ref. 130), each coupled to one of said plurality of port components (Fig. 2 Ref. 110), said cache-coherent device further including a plurality of caches (Fig. 2 Ref. 134), each coupled to one of said plurality of client ports and assigned to one of said plurality of port components, and a coherency engine (Fig. 2 Fig. 140) coupled to said plurality of caches.

As to claim 7, Shen discloses the invention as claimed in the above. Shen further discloses wherein said plurality of port components includes processor port components (Fig. 1 Ref. 110).

As to claim 8, Shen discloses the invention as claimed in the above. Shen further discloses wherein said plurality of port components includes input/output components (Fig. 1 Ref. Ref. 110).

As to claim 9, Shen discloses the invention as claimed. Shen discloses in a cache-coherent I/O device (Fig. 2) including a coherency engine (Fig. 2 Refs. 132 & 140) and a plurality of client ports (Fig. 2 Refs 130), a method for processing a transaction, comprising: receiving a transaction request (col. 7 lines 13-15) at one of said plurality of client ports on the I/O cache-coherent device, said transaction request includes an address (col. 8 line 49); and determining whether said address is present (col. 8 lines 45+) in one of a plurality of sub-unit caches (Fig. 2 Ref. 134), each of said sub-unit caches assigned to said one of said plurality of client ports (Fig. 2 Ref. 110).

As to claim 10, Shen discloses the invention as claimed in the above. Shen further discloses wherein said transaction request is a read transaction request (col. 7 lines 13-15).

As to claim 11, Shen discloses the invention as claimed in the above. Shen further discloses transmitting data for said read transaction request from said one of said plurality of sub-unit caches to one of said plurality of client ports (col. 8 lines 45+).

As to claim 12, Shen discloses the invention as claimed in the above. Shen further discloses prefetching one or more cache lines ahead of said read transaction request (cache memory reads on this limitation since the cache memory is used to assure that the currently useful data of main memory are copied into the small and fast cache for the purpose of increasing data access speed by means of spatial and temporal localities); and updating the coherency state (Col. 9 lines 5-6) information in said plurality of sub-unit caches.

As to claim 14, Shen discloses the invention as claimed in the above. Shen further discloses wherein said transaction request is a write transaction request (col. 7 lines 13-15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (Shen) U.S. Patent 6,526,481 in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp 140-240.

As to claims 5 and 13, Shen discloses the invention as claimed above. However, Shen dos not specifically disclose wherein said coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol.

However, it is well known in the cache art to using MESI cache coherency protocol for the purpose of maintaining data consistency thereby increasing the memory access speed. For example, Handy discloses coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add coherency logic protocol includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol of Handy into the invention of Shen for the advantages stated above.

As to claim 15, Shen and Handy disclose the invention as claimed in the above. Handy further discloses modifying coherency state information for a cache line in said one of said plurality of sub-unit caches; updating coherency state information in others of said plurality of sub-unit caches by said coherency engine; and transmitting data for

said write transaction request from said one of said plurality of sub-unit caches to memory (MESI protocol reads on this limitation and pages 159-161).

5. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al. (Shen) U.S. Patent 6,526,481 in view of Jim Handy, "The Cache Memory Handbook" TK7895.M4H35, 1993, pp 140-240 and further in view of Witt et al. (Witt) U.S. Patent 6,202,139.

As to claim 16, Shen further discloses modifying coherency state information of said write transaction request (col. 7 line 13-15), however, neither Shen nor Handy specifically discloses write transaction request in the order received and pipelining multiple write requests.

Witt discloses write transaction request in the order received and pipelining multiple write requests (col. 2 lines 42-43) for the purpose of avoiding bank conflicts thereby decreasing the performance losses and increasing the access speed (col. 2 lines 43-45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate write transaction request in the order received and pipelining multiple write requests as shown in Witt into the combined invention of Shen and Handy because it would avoid bank conflicts thereby decreasing the performance losses and increasing the access speed.

As to claim 17, Shen Handy and Witt disclose the invention as claimed in the above. Handy further discloses wherein the coherency state information includes a Modified-Exclusive-Shared-Invalid (MESI) cache coherency protocol (Page 159).

Response to Arguments

6. Applicant's arguments filed 8/13/04 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the use of distributed caches, the cache is pipelined and operate at a clock frequency higher than that employed by the reminder of the microprocessor including the cache for multiple accesses per clock cycle, etc) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument on page 7 that the prior arts do not disclose cache coherent I/O device has been fully considered but it is not persuasive.
Shen discloses cache coherent I/O device (Fig. 2 Ref. 130).
Therefore broadly written claims are disclosed by the references cited.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. a shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is 703-305-3835. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (571) 242-4181 The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (571) 242-4180.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

8. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Or faxed to TC-2100:
(703) 746-7238

HK
Primary Patent Examiner
October 30, 2004